

Z89314/318 DIGITAL TELEVISION CONTROLLER

FEATURES

•	Part Number Z89314 Z89318 *General-P	Z8 ROM (Kbyte) 16 10 urpose	Z8 RAM* (Kbyte) 512 512	Speed (MHz) 12 12
	40-Pin DI	P Package		
	4.5- to 5.0	-Volt Operatin	ig Range	

Z89C00 RISC Processor Core

■ 0°C to +70°C Temperature Range

- Direct Closed Caption Decoding
- TV Tuner Serial Interface
- Customized Character Set
- Character Control Mode
- Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89314/318 are members of Zilog's family of Digital Television Controllers designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The powerful Z89C00 RISC processor core allows users to control on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. This version of the Z89300 series does not offer I²C capability

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one-pixel border.

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

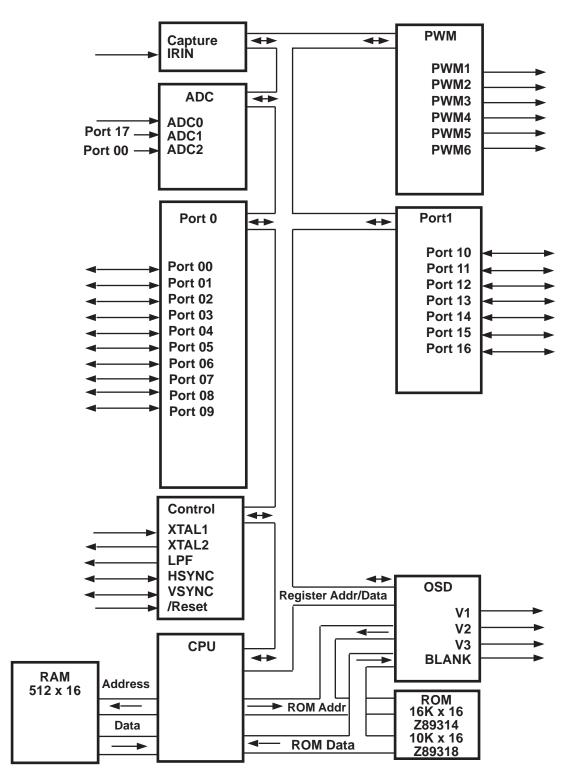
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device		
Power	V _{cc}	V _{DD}		
Ground	GND	V _{SS}		

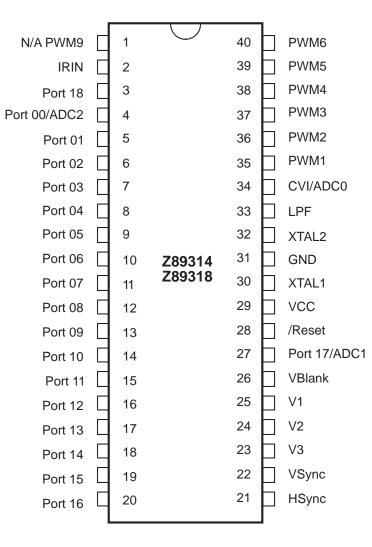
GENERAL DESCRIPTION (Continued)



Functional Block Diagram

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PIN DESCRIPTION





PIN DESCRIPTION (Continued) Z89314/318

Pin		Z89314	Configuration		
Name	Function	40-Pin	Direction	Reset	
V _{cc}	+5 V	29,-	PWR	_	
GND	0 V	31,-	PWR	-	
IRIN	Infrared Remote Capture Input	2	l		
ADC[5:0]	4-Bit Analog to Digital Converter Input	-,-,4,27,34	AI	I	
PWM[8:1] ^a 8-Bit Pulse Width Modulator Output		-,-,40,39,38 37,36,35	OD	Ο	
Port0[F:0] ^b Bit Programmable Input/Output Ports		-,-,-,-,-,-, 13,12,11 10,9,8,7,6,5,4	В	Ι	
Port1[9:0]ª	Bit Programmable Input/Output Ports	-,3,27,20, 19,18,17, 16,15,14	В	I	
XTAL1	Crystal Oscillator Input	30	AI	I	
XTAL2	Crystal Oscillator Output	32	AO	0	
LPF	Loop Filter	33	AB	0	
HSYNC	H_Sync	21	В	Ι	
VSYNC	V_Sync	22	В	1	
/RESET	Device Reset	28	Ι	Ι	
V[3:1]	OSD Video Output (Typically Drive B, G, and R Outputs)	23,24,25	0	0	
Blank	OSD Blank Output	26	0	0	
Half Blank	OSD Half Blank Output	N/A	0		
SCLK ^e	Internal Processor SCLK	20	0		

Notes:

a) PWM [8,7] is not available on the 40-pin DIP version.

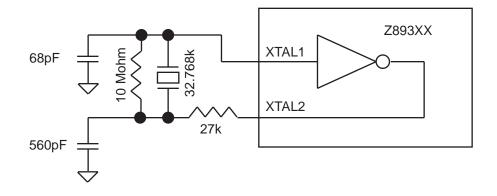
b) Port0 [F:A] is not available on the 40-pin DIP version.

c) Port19 is not available on the 40-pin DIP version.

d) Half Blank output is a function shared with PortOF.

Half Blank output is not available on the 40-pin DIP version.

e) Internal processor SCLK is shared with Port16.



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V _{cc}	Power Supply Voltage	0	7	V	
V _{ID}	Input Voltage	-0.3	V _{cc} +0.3	V	Digital Inputs
VIA	Input Voltage	-0.3	V _{cc} +0.3	V	Analog Inputs (A/D0A/D4)
Vo	Output Voltage	-0.3	V _{CC} +0.3	V	All Push-Pull Digital Output
V _o	Output Voltage	-0.3	V _{CC} +8.0	V	Open-Drain PWM Outputs
0			00		(PWM1PWM8)
I _{OH}	Output Current High		-10	mA	One Pin
I _{OH}	Output Current High		-100	mA	All Pins
I _{OL}	Output Current Low		20	mA	One Pin
	Output Current Low		200	mA	All Pins
T	Operating Temperature	0	70	°C	
T _A	Storage Temperature	-65	150	°C	

DC CHARACTERISTICS $T_A = 0^{\circ}C \text{ to } + 70^{\circ}C; V_{CC} = 4.5 \text{ V to } + 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbo	ol Parameter	Min	Max	Typical	Units	Conditions
V	Input Voltage Low	0	0.2 V _{cc}	0.4	V	
V	Input Voltage High	$0.6 V_{\rm cc}$	V _{cc}	3.6	V	
V _{PU}	Max. Pull-Up Voltage		12		V	PWM0PWM8 Only
V	Output Voltage Low		0.4	0.16	V	@ I ₀₁ = 1 mA
V _{OL} ³	Output Voltage High	$V_{\rm CC}$ –0.9		4.75	V	@ I _{oL} = 0.75 mA
V _{XL}	Input Voltage XTAL1 Low		0.3 V _{cc}	1.0	V	External Clock
V _{XH}	Input Voltage XTAL1 High	V _{cc} –2.0 3.0	00	3.5	V	Generator Driven
V _{HY} ¹	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I _{IR}	Reset Input Current		150	90	μΑ	$V_{RL} = 0 V$
I	Input Leakage	-3.0	3.0	0.01	μA	@ 0 V and V _{cc}
I _{cc}	Supply Current		100	60	mA	00
I _{CC1E} ²	Supply Current of the OTP		700	300	μΑ	Sleep Mode @ 32 KHz
I _{CC1} ²	Supply Current		300	100	μA	Sleep Mode @ 32 KHz
I _{CC2}	Supply Current		40	5	μA	Sleep Mode

Notes:

1. Not in the EOS.

2. Z89314 is not an OTP.

3. Labeled incorrect.

AC CHARACTERISTICS $T_A = 0^{\circ}C \text{ to } + 70^{\circ}C; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Мах	Typical	Units
T _P C T _R C,T _F C	Input Clock Period Clock Input Rise and Fall	16	100	32 12	μS μS
T _D POR	Power On Reset Delay	0.8		1.2	S

AC CHARACTERISTICS* $T_A = 0^{\circ}C \text{ to } + 70^{\circ}C; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
T _w RES T _D H _S	Power-On Reset Min. Width H_Sync Incoming Signal Width	5.5	5TPC 12.5	11	μS μS
$T_DV_S T_DE_S$	V_Sync Incoming Signal Width Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	0.15 -12	1.5 +12	1.0 0	mS μS
T _D O _S	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	μS
$\rm T_w HV_s$	H_Sync/V_Sync Edge Width		2.0	0.5	μS

*Notes:

The above AC Characteristics are ROM code/software dependent and are not measurable internally.

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